WHAT IS CLAIMED IS:

1. A computer system employing a pipeline operation

wherein the pipeline is driven by a high clock frequency higher than a low clock frequency by which a critical path instruction in processing data can be executed correctly, comprising:

a high frequency ALU driven by a pipeline clock frequency, a low frequency ALU driven by a low clock frequency lower than the pipeline clock frequency, by which low clock frequency the critical path instruction can be executed correctly, wherein

if the high frequency ALU can execute an instruction correctly, the execution result of the high frequency ALU is outputted as an execution result of a pipeline execution stage,

if the high frequency ALU can not execute the instruction correctly, the execution result of the low frequency ALU is outputted as an execution result of the pipeline execution stage.

2. The computer system according to claim1,

wherein the low frequency ALU is composed of plural low frequency ALUs;

the low frequency ALU in charge of each execution stage is switched in turn, and each low frequency ALU in charge executes an execution stage instruction in charge correctly by the low clock frequency which is equal to or lower than the clock frequency for operating a critical path instruction correctly.

3. The computer system according to claim 2,

wherein the number of the plural low frequency ALUs is "n" when the pipeline clock frequency is "n" times of the clock frequency by which the critical path instruction can be executed correctly,

each of the "n" pieces of the low frequency ALUs is in charge of "n" pieces of execution stages of pipeline in order respectively.

4. The computer system according to claim 3, further comprising a comparator comparing the output of the high frequency ALU and the output of the low frequency ALU in charge of the same execution stage for the same instruction,

wherein, the output of the high frequency ALU is assumed as the execution result of the pipeline execution stage, and when the compared result of the comparator indicates matching, the output of the high frequency ALU is determined as the execution result of the execution stage and the pipeline operation is continued, and when the

compared result of the comparator indicates mismatching, the output of the high frequency ALU is replaced with the output of the low frequency ALU as the execution result of the pipeline execution stage.

5. The computer system according to claim 4, wherein when the compared result of the comparator indicates mismatching, all stages of the pipeline are stopped until finishing the replacement process in which the output of the low frequency ALU is selected as the execution result of the pipeline execution stage.

6. The computer system according to claim 2, further comprising a comparator comparing the output of the high frequency ALU and the output of the low frequency ALU in charge of the same execution stage for the same instruction,

wherein, the output of the high frequency ALU is assumed as the execution result of the pipeline execution stage, and when the compared result of the comparator indicates matching, the output of the high frequency ALU is determined as the execution result of the execution stage and the pipeline operation is continued, and when the compared result of the comparator indicates mismatching, the output of the high frequency ALU is replaced with the output of the low frequency ALU as the execution result of the pipeline execution stage.

7. The computer system according to claim 6, wherein when the compared result of the comparator indicates mismatching, all stages of the pipeline are stopped until finishing the replacement process in which the output of the low frequency ALU is selected as the execution result of the pipeline execution stage.

8. The computer system according to claim 1 further comprising a comparator comparing the output of the high frequency ALU and the output of the low frequency ALU in charge of the same execution stage for the same instruction,

wherein, the output of the high frequency ALU is assumed as the execution result of the pipeline execution stage, and when the compared result of the comparator indicates matching, the output of the high frequency ALU is determined as the execution result of the execution stage and the pipeline operation is continued, and when the compared result of the comparator indicates mismatching, the output of the high frequency ALU is replaced with the output of the low frequency ALU as the execution result of the pipeline execution stage.

9. The computer system according to claim 8, wherein when the compared result of the

comparator indicates mismatching, all stages of the pipeline are stopped until finishing the replacement process in which the output of the low frequency ALU is selected as the execution result of the pipeline execution stage.

10. The computer system according to claim 1, further comprising a counter counting the number of occurrences of the mismatching detection signal in a predetermined period, and a circuit varying the pipeline clock frequency according to the counted number.

11. The computer system according to claim 1 wherein the following amounts of two processes are compared when the pipeline clock frequency is increased and the number of the critical path instructions is increased, the one being an improved process amount of the high frequency ALU and the other being a deteriorated process amount by increasing of the replacement process of the output of the low frequency ALU as the execution result of the pipeline execution stage when the high frequency ALU cannot execute the instruction correctly,

wherein, when the former is larger than the latter by the predetermined amount, the pipeline clock frequency is increased.

12. The computer system according to claim 1 wherein, the following amounts of two processes are compared when the pipeline clock frequency is decreased and the number of the critical path instructions is decreased, the one being a deteriorated process amount of the high frequency ALU if the pipeline clock frequency is lowered, and the other being an improved process amount by decreasing of the replacement process of the output of the low frequency ALU as the execution result of the pipeline execution stage when the high frequency ALU cannot execute the instruction correctly,

wherein, when the latter is larger than the former by a predetermined amount, the pipeline clock frequency is decreased.

13. The computer system according to claim 1 further comprising plural ALUs, a data generation circuit generating test data as a critical path data, an execution time measurement circuit measuring critical path instruction in each ALU, and a detector detecting the fastest ALU that can execute the critical path instruction in a shortest time,

wherein, the ALU detected by the detector is selected as the high frequency ALU, and the other one ALU or plural ALUs is/are selected as the low frequency ALU/ALUs.

14. A method for controlling a pipeline operation in a computer system

wherein the pipeline is driven by a high clock frequency higher than a low clock

frequency by which a critical path instruction in processing data can be executed correctly, comprising:

using a high frequency ALU driven by a pipeline clock frequency, a low frequency ALU driven by a low clock frequency lower than the pipeline clock frequency, by which low clock frequency the critical path instruction can be executed correctly, wherein

if the high frequency ALU can execute an instruction correctly, outputting the execution result of the high frequency ALU as an execution result of a pipeline execution stage,

if the high frequency ALU can not execute the instruction correctly, outputting the execution result of the low frequency ALU as an execution result of the pipeline execution stage.

15. The method for controlling a pipeline operation in a computer system according to claim14,

wherein the low frequency ALU is composed of plural low frequency ALUs;

switching the low frequency ALU in charge of each execution stage in turn, and assigning each low frequency ALU in charge for an execution stage instruction in charge to execute it correctly by the low clock frequency which is equal to or lower than the clock frequency for operating a critical path instruction correctly.

16. The method for controlling a pipeline operation in a computer system according to claim 15,

wherein the number of the plural low frequency ALUs is "n" when the pipeline clock frequency is "n" times of the clock frequency by which the critical path instruction can be executed correctly,

each of the "n" pieces of the low frequency ALUs is in charge of "n" pieces of execution stages of pipeline in order respectively.

17. The method for controlling a pipeline operation in a computer system according to claim 16, further comprising comparing method for comparing the output of the high frequency ALU and the output of the low frequency ALU in charge of the same execution stage for the same instruction,

wherein, the output of the high frequency ALU is assumed as the execution result of the pipeline execution stage, and when the compared result indicates matching, the output of the high frequency ALU is determined as the execution result of the execution stage and the pipeline operation is continued, and when the compared result

indicates mismatching, the output of the high frequency ALU is replaced with the output of the low frequency ALU as the execution result of the pipeline execution stage.

18. The method for controlling a pipeline operation in a computer system according to claim 17, wherein when the compared result indicates mismatching, all stages of the pipeline are stopped until finishing the replacement process in which the output of the low frequency ALU is selected as the execution result of the pipeline execution stage.

19. The method for controlling a pipeline operation in a computer system according to claim 15, further comprising a comparing method for comparing the output of the high frequency ALU and the output of the low frequency ALU in charge of the same execution stage for the same instruction,

wherein, the output of the high frequency ALU is assumed as the execution result of the pipeline execution stage, and when the compared result indicates matching, the output of the high frequency ALU is determined as the execution result of the execution stage and the pipeline operation is continued, and when the compared result indicates mismatching, the output of the high frequency ALU is replaced with the output of the low frequency ALU as the execution result of the pipeline execution stage.

20. The method for controlling a pipeline operation in a computer system according to 19, wherein when the compared result indicates mismatching, all stages of the pipeline are stopped until finishing the replacement process in which the output of the low frequency ALU is selected as the execution result of the pipeline execution stage.

21. The method for controlling a pipeline operation in a computer system according to claim 14 further comprising a comparing method for comparing the output of the high frequency ALU and the output of the low frequency ALU in charge of the same execution stage for the same instruction,

wherein, the output of the high frequency ALU is assumed as the execution result of the pipeline execution stage, and when the compared result indicates matching, the output of the high frequency ALU is determined as the execution result of the execution stage and the pipeline operation is continued, and when the compared result indicates mismatching, the output of the high frequency ALU is replaced with the output of the low frequency ALU as the execution result of the pipeline execution stage.

22. The method for controlling a pipeline operation in a computer system according to claim 21, wherein when the compared result indicates mismatching, all stages of the

pipeline are stopped until finishing the replacement process in which the output of the low frequency ALU is selected as the execution result of the pipeline execution stage.

23. The method for controlling a pipeline operation in a computer system according to claim 14, further comprising a counting method for counting the number of occurrences of the mismatching detection signal in a predetermined period, and a method for varying the pipeline clock frequency according to the counted number.

24. The method for controlling a pipeline operation in a computer system according to claim 14 wherein the following amounts of two processes are compared when the pipeline clock frequency is increased and the number of the critical path instructions is increased, the one being an improved process amount of the high frequency ALU and the other being a deteriorated process amount by increasing of the replacement process of the output of the low frequency ALU as the execution result of the pipeline execution stage when the high frequency ALU cannot execute the instruction correctly,

wherein, when the former is larger than the latter by the predetermined amount, the pipeline clock frequency is increased.

25. The method for controlling a pipeline operation in a computer system according to claim 14 wherein, the following amounts of two processes are compared when the pipeline clock frequency is decreased and the number of the critical path instructions is decreased, the one being a deteriorated process amount of the high frequency ALU if the pipeline clock frequency is lowered, and the other being an improved process amount by decreasing of the replacement process of the output of the low frequency ALU as the execution result of the pipeline execution stage when the high frequency ALU cannot execute the instruction correctly,

wherein, when the latter is larger than the former by a predetermined amount, the pipeline clock frequency is decreased.

26. The method for controlling a pipeline operation in a computer system according to claim 14, using plural ALUs, further comprising a method for generating test data as a critical path data, a method for measuring critical path instruction in each ALU, and a method for detecting the fastest ALU that can execute the critical path instruction in a shortest time,

wherein, the detected ALU is selected as the high frequency ALU, and the other one ALU or plural ALUs is/are selected as the low frequency ALU/ALUs.